

## AMENDMENTS TO THE SPECIFICATION:

Please add the paragraph beginning between the paragraphs [0029] and the heading, "DETAILED DESCRIPTION OF THE INVENTION."

--FIG. 15 illustrates (through cross-sectional view) another embodiment of the memory array of the present invention comprising a further-offset buried strap.--

Please add the paragraph beginning between paragraphs [0068] and [0069]:

-- Referring to FIG. 15, another memory array according to another embodiment of the present invention includes at least one other-type memory device 23, each of the at least one other-type memory device 23 comprising another transistor 10', another underlying capacitor 20', a further-offset buried strap 15', and another collar region 25 with another vertical length L5, wherein the further-offset buried strap 15' is located at another depth that is different from the first depth and from the second depth and is positioned on the another collar region and is in electrical contact with both the another transistor and the another underlying capacitor, and the another vertical length L5 is equal to the first vertical length L3. The structure of the another memory array containing the at least one other-type memory device is formed by repeated applications of the methods described above that is used to differentiate the depth of the first-type memory trench device 21 and the second-type memory trench device 22.--